WHAT IS CLAIMED IS:

1. A charge detection device comprising:

a charge detection node;

a buffer amplifier having an input coupled to the charge detection node;

a reset switch coupled to the charge detection node;

a feedback capacitor having a first end coupled to the charge detection node;

a holding capacitor having a first end coupled to a second end of the feedback capacitor; and

a feedback amplifier having a first input coupled to an output of the buffer amplifier and an output coupled to the second end of the feedback capacitor.

2. The device of claim 1 further comprising a feedback switch coupled between the output of the feedback amplifier and the second end of the feedback capacitor.

3. The device of claim 2 further comprising a first switch coupled between the output of the feedback amplifier and a second end of the holding capacitor.

4. The device of claim 3 further comprising a second switch coupled between a second input of the feedback amplifier and the second end of the holding capacitor, wherein

the second switch is clocked in phase with the feedback switch.

5. The device of claim 4 further comprising a reference voltage node coupled to the second input of the feedback amplifier.

6. The device of claim 1 wherein the feed back amplifier has a variable gain level.

7. The device of claim 6 further comprising a processing device having an input coupled to the output of the buffer amplifier and an output coupled to a gain control node of the feedback amplifier, wherein the processing device controls the variable gain level of the feedback amplifier.

8. The device of claim 7 wherein the variable gain level of the feedback amplifier is set in predetermined time intervals to values determined by the processing device.

9. The device of claim 8 wherein the processing device comprises a memory from which the variable gain level is determined.

10. The device of claim 9 wherein the processing device further comprises a digital signal processor for computing the variable gain level.

11. The device of claim 10 wherein the processing device further comprises an analog-to-digital converter coupled between the output of the buffer amplifier and the digital signal processor.

12. The device of claim 6 wherein the variable gain level is periodically changed within predetermined pulse intervals that are in correlation with charge arriving on the charge detection node.

13. The device of claim 2 wherein the feedback amplifier is shared by all charge detection nodes in one column, wherein the charge detection nodes are reset and addressed by pulses supplied through row addressing lines and the feedback switch is addressed by pulses supplied through the row addressing lines.

14. The device of claim 2 wherein the feedback transistor is addressed by pulses supplied through a column addressing line.